Amendment to the Claims:

Please cancel claim 1, amend claims 2, 4-5 and 11 and add claims 12-20 as follows:

1. (Cancelled)

2. (Currently amended) A viewfinder apparatus for a television camera, comprising a display device using a video signal processing circuit as set forth in Claim ~~1~~ 12.

3. (Original) A television camera comprising a viewfinder apparatus as set forth in Claim 2.

4. (Currently amended) An image monitor apparatus comprising a display device using a video signal processing circuit as set forth in Claim ~~1~~ 12.

5. (Currently amended) The video signal processing circuit as set forth in Claim ~~1~~ 12, wherein the contour-~~adjustment~~adjusting circuit further comprises at least one peaking circuit ~~that peaks~~ configured to peak either the R, G and B signals from video signals in one of ~~the~~ a NTSC system and ~~the~~ a PAL system or ~~that peaks~~ only the Y signal from transmission color signals in ~~the~~ a high definition television system.

6. (Previously presented) The video signal processing circuit as set forth in Claim 5, wherein the at least one peaking circuit receives as an input the R, G or B signal from video signals in one of the NTSC system and the PAL system.

7. (Previously presented) The video signal processing circuit as set forth in Claim 5, wherein one peaking circuit receives as an input the Y signal from transmission color signals in the high definition television system.

8. (Previously presented) The video signal processing circuit as set forth in Claim 7, wherein the Pr signal and the Pb signal are directly inputted to the inverse matrix transforming circuit.

9. (Previously presented) The video signal processing circuit as set forth in Claim 6, wherein each peaking circuit includes at least one delay circuit that delays the input signal and delayed signals; at least one subtractor that subtracts delayed signals from the input signal, at least one adder that adds subtracted signals, at least one amplifier that amplifies added signals, and an appending circuit that appends the delayed signals to amplified signals to form a peaked signal.

10. (Previously presented) The video signal processing circuit as set forth in Claim 7, wherein each peaking circuit includes at least one delay circuit that delays the input signal and delayed signals; at least one subtractor that subtracts delayed signals from the input signal, at least one adder that adds subtracted signals, at least one amplifier that amplifies added signals, and an appending circuit that appends the delayed signals to amplified signals to form a peaked signal.

11. (Currently amended) The video signal processing circuit as set forth in Claim ~~1~~ 12, further comprising a determining unit producing a control signal, wherein in response to the control signal, the selecting circuit changes selection of ~~the~~ at least one switch to relay either the R, G, and B signals in which the contour adjustment is performed or the Y signal, in which the contour adjustment is performed, and the Pr signal and the Pb signal, in which the contour adjustment is not performed.

12. (New) A video signal processing circuit, comprising:

an input terminal receiving one of NTSC video signals, PAL video signals and high definition television transmission color signals;

a contour-adjusting circuit configured to receive one of the NTSC video signals, the PAL video signals and the high definition television transmission color signals from the input terminal and peak the received signals for contour adjustment;

an inverse matrix transforming circuit for separating R, G and B signals from the high definition television transmission color signals;

a selecting circuit that controls adjusted NTSC video signals and adjusted PAL signals to bypass the inverse matrix transforming circuit; and,

an output terminal outputting video signals that include contour-adjusted R, G and B signals.

13. (New) A video signal processing circuit operable in an NTSC system, a PAL system and a high definition television system, comprising:

at least one peaking processing circuit;

an inverse matrix transforming circuit; and,

wherein R, G and B signals from video signals in one of the NTSC system and the PAL system are inputted into the peaking processing circuit and are contour-adjusted by the peaking processing circuit and are outputted as first output signals, and

wherein a Y signal from transmission color signals in the high definition television system is inputted into the peaking processing circuit and is contour-adjusted by the peaking processing circuit, and an adjusted Y signal, an unadjusted Pr signal and an unadjusted Pb signal from the transmission color signals are inputted into the inverse matrix transforming circuit so as to separate R, G and B signals therefrom and output the separated R, G and B signals as second output signals.

14. (New) A video signal processing circuit, comprising:

an input terminal inputting one of NTSC video signals, PAL video signals and high definition television transmission color signals, wherein the NTSC video signals and the PAL video signals include R, G and B signals and the high definition television transmission color signals include a Y signal, a Pr signal and a Pb signal; and

a contour-adjusting circuit configured to receive one of the NTSC video signals, the PAL video signals and the high definition television transmission color signals from the input terminal and peak the received signals for contour adjustment; and

an inverse matrix transforming circuit for separating R, G and B signals from an adjusted Y signal, the Pr signal and the Pb signal;

wherein the contour-adjusting circuit is operable to process the R, G and B signals in one of a NTSC system and a PAL system and the Y signal in a high definition television system.

15. (New) The video signal processing circuit as set forth in Claim 14, wherein the Pr signal and the Pb signal bypass the contour-adjusting circuit and are directly inputted into the inverse matrix transforming circuit.

16. (New) The video signal processing circuit as set forth in Claim 14, further comprising a selecting circuit that selects circuit connection in accordance with the type of input signals.

17. (New) The video signal processing circuit as set forth in Claim 16, further comprising a plurality of selecting switches configured to be driven simultaneously by the selecting circuit.

18. (New) The video signal processing circuit as set forth in Claim 17, wherein at least one selecting switch includes at least two input terminals, a first input terminal configured to receive one of the NTSC video signals and the PAL video signals and a second input terminal configured to receive the high definition television transmission signals.

19. (New) The video signal processing circuit as set forth in Claim 18, wherein in accordance with the type of input signals, the selecting circuit drives the selecting switch to connect one of the first input terminal and the second input terminal to an output terminal.

20. (New) The video signal processing circuit as set forth in Claim 19, wherein in response to one of the NTSC video signals and the PAL video signals, the selecting circuit drives the first input terminal of the selecting switch to be connected to the output terminal, and in response to the high definition television transmission signal, the selecting circuit drives the second input terminal of the selecting switch to be connected to the output terminal.